CLAIMS

Please amend the claims as follows:

1.-5. (canceled)

6. (currently amended) A method of preparing a simulation model of an electronic design within a data processing system, said method comprising:

receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic design, wherein the plurality of design entities includes a plurality of signals[[,]] and functional logic~~, and any storage elements~~ that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, said one or more statements including a trace array declaration conforming to predetermined syntax, said trace array declaration containing at least:

a keyword declaring existence of ~~specifying~~ a trace array within the instrumentation entity[[,]]; and ~~indicating~~

an indication of a monitored signal set including at least one signal among the plurality of signals; and

in response to receipt of the one or more HDL files, parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array is configured to concurrently store multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

~~wherein said parsing and processing said one or more HDL files includes:~~

~~creating, within the trace array, storage for multiple values of the monitored signal set;~~

~~creating an association between an enumerated value and a value of the at least one signal comprising said monitored signal set; and~~

placing the simulation model in data storage.

7.-11. (canceled)

12. (currently amended) A method of reporting simulation data obtained by the simulation of an electronic design within a data processing system, said method comprising:

a simulator running a testcase against a simulation model of the electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals[[,]] and functional logic~~, and any storage elements~~ that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein recording trace data includes recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted; and

exporting said trace data from said trace array in a trace file and storing said trace file in data storage~~, wherein exporting the trace data in a trace file includes exporting the trace data in a~~

~~trace file indicating an association between an enumerated value and a value of said monitored signal set.~~

13.-20. (canceled)

21. (currently amended) A data processing system for preparing a simulation model of an electronic design, said data processing system comprising:

means for receiving one or more hardware description language HDL files declaring a plurality of design entities forming the digital design, wherein the plurality of design entities includes a plurality of signals[[,]] and functional logic~~, and any storage elements~~ that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, said one or more statements including a trace array declaration conforming to predetermined syntax, said trace array declaration containing at least:

a keyword declaring existence of ~~specifying~~ a trace array within the instrumentation entity[[,]]; and ~~indicating~~

an indication of a monitored signal set including at least one signal among the plurality of signals; and

means, responsive to receipt of the one or more HDL files, for parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model~~, wherein said means for parsing and processing said one or more HDL files includes means for creating an association between an enumerated value and a value of the at least one signal comprising said monitored signal set~~; and

means for storing the simulation model in data storage.

22.-26. (canceled)

27. (currently amended) A data processing system, comprising:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals[[,]] and functional logic~~, and any storage elements~~ that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein recording trace data includes recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage~~, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between an enumerated value and a value of said monitored signal set~~.

28.-35. (canceled)

36. (currently amended) An apparatus for preparing a simulation model of an electronic design, said apparatus comprising:

a tangible computer usable medium containing program code, said program code including:

~~means~~ instructions for receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic design, wherein the plurality of design entities includes a plurality of signals[[,]] and functional logic~~, and any storage elements~~ that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, said one or more statements including a trace array declaration conforming to predetermined syntax, said trace array declaration containing at least:

a keyword declaring existence of ~~specifying~~ a trace array within the instrumentation entity[[,]]; and ~~indicating~~

an indication of a monitored signal set including at least one signal among the plurality of signals; and

instructions ~~means~~, responsive to receipt of the one or more HDL files, for parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model~~, wherein said means for parsing and processing said one or more HDL files includes means for creating an association between an enumerated value and a value of said monitored signal set~~; and

instructions for storing the simulation model in data storage.

37.-41. (canceled)

42. (currently amended) An apparatus comprising:

a computer usable medium containing program code, said program code including:

instructions ~~means~~ for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals[[,]] and functional logic~~, and any storage elements~~ that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals; and

instructions ~~means~~ for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein recording trace data includes recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted; and

instructions ~~means~~ for exporting said trace data from said trace array in a trace file and storing said trace file in data storage~~, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between an enumerated value and a value of said monitored signal set~~.

43.-45. (canceled)

46. (new) The method of Claim 6, wherein said receiving further comprises receiving in said trace array declaration an identification of a control signal among said plurality of signals, wherein values assumed by said monitored signal set are stored within the trace array only on those cycles of functional operation during which the control signal is asserted and are not stored on those cycles of functional operation during which the control signal is not asserted.

47. (new) The method of Claim 6, wherein parsing and processing said one or more HDL files further comprises parsing and processing the trace array declaration to create within the simulation model an association between a value of the at least one signal comprising said monitored signal set and an enumerated value containing a textual string.

48. (new) The method of Claim 6, wherein said trace array declaration includes a keyword specifying a particular type for the trace array among a plurality of different types of trace arrays.

49. (new) The method of Claim 6, wherein said receiving comprises receiving the trace array declaration within an HDL file declaring at least one of said plurality of design entities.

50. (new) The method of Claim 6, wherein said parsing and processing includes automatically replicating said trace array within a plurality of instances of a design entity declared by an HDL file containing the trace array declaration.

51. (new) The method of Claim 6, wherein said receiving comprises receiving said trace array declaration in a comment in the one or more HDL files.

52. (new) The method of Claim 12, wherein exporting the trace data in a trace file includes exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

53. (new) The method of Claim 12, wherein recording trace data comprises recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set.

54. (new) The method of Claim 53, wherein:

the trace array has a counter that counts the functional cycles; and

said recording trace data includes recording in the trace array an entry indicating overflow of said counter.

55. (new) The method of Claim 12, and further comprising:

during function operation, the instrumentation entity signaling that the trace array is full;

in response to said signaling, automatically halting running of the testcase prior to completion of the testcase and performing said exporting; and

thereafter, resuming running of the testcase.

56. (new) The method of Claim 12, wherein said exporting includes:

exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

57. (new) The method of Claim 12, wherein said storing comprises:

for each of a plurality of simulation runs, grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

58. (new) The method of Claim 12, wherein said storing comprises automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

59. (new) The method of Claim 12, and further comprising accessing the trace file in data storage with a trace analysis tool.

60. (new) The data processing system of Claim 21, wherein said means for receiving further comprises means for receiving in said trace array declaration an identification of a control signal

among said plurality of signals, wherein values assumed by said monitored signal set are stored within the trace array only on those cycles of functional operation during which the control signal is asserted and are not stored on those cycles of functional operation during which the control signal is not asserted.

61. (new) The data processing system of Claim 21, wherein said means for parsing and processing said one or more HDL files further comprises means for parsing and processing the trace array declaration to create within the simulation model an association between a value of the at least one signal comprising said monitored signal set and an enumerated value containing a textual string.

62. (new) The data processing system of Claim 21, wherein said trace array declaration includes a keyword specifying a particular type for the trace array among a plurality of different types of trace arrays.

63. (new) The data processing system of Claim 21, wherein said means for receiving comprises means for receiving the trace array declaration within an HDL file declaring at least one of said plurality of design entities.

64. (new) The data processing system of Claim 21, wherein said means for parsing and processing includes means for automatically replicating said trace array within a plurality of instances of a design entity declared by an HDL file containing the trace array declaration.

65. (new) The data processing system of Claim 21, wherein said means for receiving comprises means for receiving said trace array declaration in a comment in the one or more HDL files.

66. (new) The data processing system of Claim 27, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

67. (new) The data processing system of Claim 27, wherein said means for recording trace data comprises means for recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set.

68. (new) The data processing system of Claim 67, wherein:

the trace array has a counter that counts the functional cycles; and

said means for recording trace data includes means for recording in the trace array an entry indicating overflow of said counter.

69. (new) The data processing system of Claim 27, and further comprising:

means for detecting signaling by the instrumentation entity during function operation that the trace array is full;

means, responsive to said signaling, for automatically halting running of the testcase prior to completion of the testcase; and

means for resuming running of the testcase after exporting said trace data.

70. (new) The data processing system of Claim 27, wherein said means for exporting includes:

means for exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

71. (new) The data processing system of Claim 27, wherein said means for storing comprises:

means, for each of a plurality of simulation runs, for grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

72. (new) The data processing system of Claim 27, wherein said means for storing comprises means for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

73. (new) The data processing system of Claim 27, and further comprising a trace analysis tool for accessing the trace file in data storage.

74. (new) The apparatus of Claim 36, wherein said instructions for receiving further comprises instructions for receiving in said trace array declaration an identification of a control signal among said plurality of signals, wherein values assumed by said monitored signal set are stored within the trace array only on those cycles of functional operation during which the control signal is asserted and are not stored on those cycles of functional operation during which the control signal is not asserted.

75. (new) The apparatus of Claim 36, wherein said instructions for parsing and processing said one or more HDL files further comprises instructions for parsing and processing the trace array declaration to create within the simulation model an association between a value of the at least one signal comprising said monitored signal set and an enumerated value containing a textual string.

76. (new) The apparatus of Claim 36, wherein said trace array declaration includes a keyword specifying a particular type for the trace array among a plurality of different types of trace arrays.

77. (new) The apparatus of Claim 36, wherein said instructions for receiving comprises instructions for receiving the trace array declaration within an HDL file declaring at least one of said plurality of design entities.

78. (new) The apparatus of Claim 36, wherein said instructions for parsing and processing includes instructions for automatically replicating said trace array within a plurality of instances of a design entity declared by an HDL file containing the trace array declaration.

79. (new) The apparatus of Claim 36, wherein said instructions for receiving comprise instructions for receiving said trace array declaration in a comment statement in the one or more HDL files.

80. (new) The apparatus of Claim 42, wherein the instructions for exporting the trace data in a trace file include instructions for exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

81. (new) The apparatus of Claim 42, wherein instructions for recording trace data comprise instructions for recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set.

82. (new) The apparatus of Claim 81, wherein:

the trace array has a counter that counts the functional cycles; and

said instructions for recording trace data include instructions for recording in the trace array an entry indicating overflow of said counter.

83. (new) The apparatus of Claim 42, and further comprising:

instructions for detecting signaling during function operation by the instruction entity that the trace array is full;

instructions, in response to said signaling, for automatically halting running of the testcase prior to completion of the testcase and performing said exporting; and

thereafter, resuming running of the testcase.

84. (new) The apparatus of Claim 42, wherein said instructions for exporting include:

instructions for exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

85. (new) The apparatus of Claim 42, wherein said instructions for storing comprise:

instructions that, for each of a plurality of simulation runs, group all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

86. (new) The apparatus of Claim 42, wherein said instructions for storing comprises instructions for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

87. (new) The apparatus of Claim 42, and further comprising a trace analysis tool for accessing the trace file in data storage.